UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,170	01/21/2004	Joong-Eon Lee	8836-228 (IB12295-US)	3742

22150 7590 03/10/2006

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
DOAN, DUC T	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,170	LEE ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-12 are in the application.

Claims 1-12 are rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5,7-11 rejected under 35 U.S.C. 103(a) as being unpatentable over Dalrymple (US 4942553) and in view of Kang (US 6748497).

As in claim 1, Dalrymple describes a computer system comprising: a digital signal processing (DSP) core for processing data in accordance with an instruction (Fig 2: #102 microprocessor, as a master processor decodes instruction and provide necessary steps to a co-processor); a data cache for storing temporary data associated with the DSP core; a first buffer module for storing input data received by the DSP core (Fig 2: #112 transmitter, receiving data

from an external memory and transmitting to the processor and co-processor); a second buffer module for storing output data provided from the DSP core(Fig 2: #112 receiver, receiving data from the processor and co-processor and transmitting to an external memory); and an external memory for storing the temporary data, the input data, and the output data (Fig 2: #106). Dalrymple does not explicitly describe a data cache. However, Kang describes a system on a chip (Kang's Fig 2: #102 SOC) having microprocessor core (Kang's Fig 2: #128 corresponds to the claim's DSP core) and cache memory (Kang's Fig 2: #126, column 3 lines 53-65). It would have been obvious to one of ordinary skill in the art at the time of invention to include the cache memory as suggested by Kang in Dalrymple's system thereby providing a fast access to data stored in the cache.

As in claim 2, the claim recites wherein the first and second buffer modules comprise: an address buffer for storing an address of the external memory; an increment unit for increasing the address by one bit; a buffer for storing either the input data or the output data; and a multiplexer for addressing the buffer in response to lower bits of the address. Dalrymple does not explicitly describe the claim's detail of addressing buffer. However, Kang clearly describes using the address of the external memory in the read or write transaction and multiplex to point to the appropriate buffers in column 6 line 40 to column 7 line 4. Furthermore, in order to point to the next location in the buffer, it's obviously an incrementing circuit is required.

As in claim 3, the claim recites wherein the address of the external memory is initialized by a central processing unit (CPU) core. The claim rejected based on the same rationale as in the rejection of claim 2. Dalrymple further describes the co-processor (corresponds to the claim's

CPU core) initiates the filling buffer operation by sending a request to the DMA engine (Dalrymple's column 4 lines 28-43).

As in claim 4, the claim recites wherein the buffer comprises a set of data registers. Dalrymple does not describe the claim's buffer aspect of data registers However, Kang describes the buffer includes set of registers in column 8 lines 13-30.

As in claim 5, the claim recites wherein the buffer comprises valid bits that inform of current occupation state by data in the data registers. The claim rejected based on the same rationale as in the rejection of claim 4. Kang's column 11 lines 1-10 describe the valid bit for each register.

As in claims 7-8, the claims recite wherein when the buffer is empty, a CPU core carries out a pre-fill operation to serially read the input data from the external memory and stack the input data in the buffer (claim 7); wherein when the buffer is full, a CPU carries out a post-flush operation to store the output data of the buffer in the external memory (claim 8). Dalrymple describes the coprocessor circuits detects the fill level exceeding the interrupt request level, therefore it initiates the "flush" operation to prevent the buffer overrun. Similarly the "fill" operation is described in Dalrymple's column 6 lines 23-43. Dalrymple's column 4 lines 24-48 describe similar operations for DMA to control data from memory into FIFO or from FIFO into memory.

As in claims 9-10, the claims recite wherein an auto-fill operation is carried out by the buffer module to stack the input data of the external memory in the buffer when the buffer is empty (claim 9); wherein if the buffer is full, the buffer module carries out an auto-flush operation to store the output data of the buffer in the external memory. (claim 10). Dalrymple

describes the coprocessor circuits detects the fill level exceeding the DMA request level, it initiates a "fill" operation to obtain more data to be transferred from memory to FIFO. Dalrymple's column 4 lines 24-48 describe similar operations for DMA to control data from memory into FIFO or from FIFO into memory.

As in claim 11, the claim recites wherein the computer system is integrated on a chip, comprising a CPU core, the DSP core, the data cache, and the first and second buffer modules. The claim rejected based on the same rationale as in the rejection of claim 1.

Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Dalrymple et al (US 4942553,) Kang et al (US 6748497) as applied to claim 1, and further in view of Hellman et al (US 6912638).

As in claim 6, the claim recites wherein the external memory comprises a temporary data field, an input data field, and an output data field, which are independently arranged therein. Dalrymple and Kang do not describe the claim's detail of arraignment the external memory. However, Hellman describes a system on chip controller in which the data in the system memory (corresponds to the claim's external memory) are segmented into arbitrary rows and columns of data (Hellman's column 8 lines 18-32). The data in these rows and columns are further grouped and distributing to local memory of DSP processors in a manner, for example a group for transferring using inbound access channel (Hellman's Fig 5A: #510), outbound access channel (Hellman's Fig 5A: #520), the data in the system memory can be in a group that is shared among processors (Hellman's column 8 lines 5-20). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory access controller and methods as

suggested by Hellman in Dalrymple's system advantaging to provide accessing the data in parallel, thereby increase the system's overall throughput.

Claim 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Dalrymple et al (US 4942553,) Kang et al (US 6748497) and further in view of Hellman et al (US 6912638).

As for claim 12, the claim recites a method of accessing data in a computer system having a digital signal processing (DSP) core, a data cache, a buffer, and an external memory, comprising the steps of: accessing temporary data for the external memory through the data cache if data of the DSP core includes the temporary data; executing a pre-fill operation to serially transfer input data to the buffer when the buffer is empty; executing a post-flush operation to store output data of the buffer in the external memory when the buffer is full; executing an auto-fill operation to stack the input data of the external memory in the buffer when the buffer is empty; and executing an auto-flush operation to store the output data of the buffer in the external memory when the buffer is full. The claim rejected based on the same rationale as in the rejections of claims 1, 6, and 7-10.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DD

Mano Padmanabhan

Supervisory Patent Examiner

TC2188

Mano Padmanabhan 3/2/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER